INSTRUCTION MANUAL

MODEL 2099-42 CLOCK GENERATOR

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TABLE OF CONTENTS **PAGE**

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MODEL 2099-42 CLOCK GENERATOR

SECTION 1 GENERAL

1.1 Equipment Description- The Model 2099-42 Clock Generator provides two RS422 clock signals selectable from 256, 192, 128, 96 or 64 kHz locked to an external 10 MHz reference and generated from a 12.288 MHz VCXO. Level detection circuitry provides an alarm signal if the external 10 MHz signal is removed and automatic switching tunes the VCXO in the PLL to 12.28800 MHz until the 10 MHz clock is restored. LEDs indicate PLL and Level alarms, Manual operation, and selection of internal or external (lock to 10 MHz) control of the VCXO. A front panel switch manually selects internal or external (lock to 10 MHz) control of the VCXO. Diodes on the DC inputs allow operation from redundant power supplies. An open collector indicates Manual operation and relay contacts indicate a major alarm due to loss of PLL lock or 10 MHz reference. The unit is housed in an aluminum extrusion chassis and can be mounted on an 1 3/4", rack panel (Option -R). A 115 VAC wall power supply provides DC power to the 2099-42.

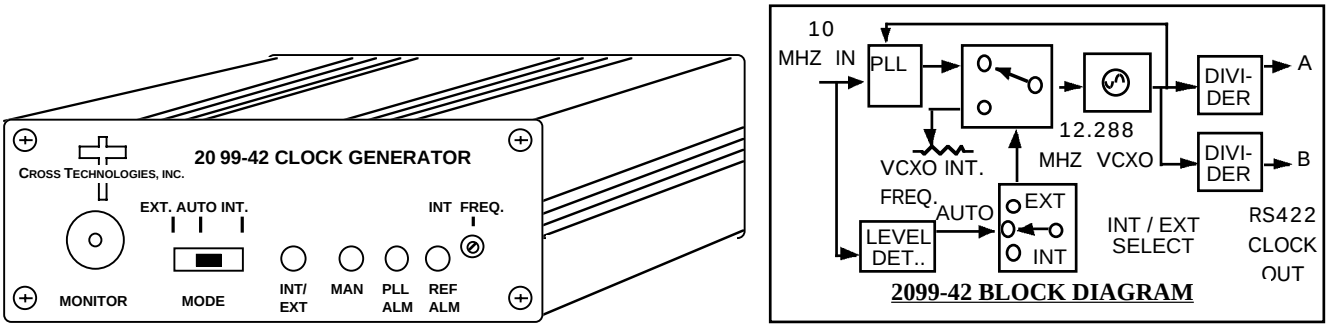

FIGURE 1.1 2099-42 Clock Generator Block Diagram and Front Panel

1.2 Technical Characteristics

TABLE 1.0 2099-42 CLOCK GENERATOR SPECIFICATIONS

Characteristics	Specifications*
10 MHz Input Characteristics	
Input level	0.5 TO 1.5 V P-P (-4 to +6 dBm into 75 ohms),
Input Impedance	75 Ω or > 2 KΩ, selectable
Clock Output Characteristics	
Level	RS422
Data Rate	64, 96, 128, 192, 256 kB/s selectable, 2 separate outputs
Stability, Ext Ref.	Same as reference
Stability, Int. Ref.	± 50 ppm
Jitter	≤ 1 degree
Controls and Indicators	
Int/AUTO/Ext Switch	Switches between internal and external (lock to 10 MHz) control of VCXO or AUTO select
Int. Freq	Adjusts frequency of internal VCXO when not locked to external 10 MHz
INT/EXT LED	LED lights RED if VCXO controlled internally, Green if locked to external 10 MHz
MAN. LED	LED lights RED when Int/AUTO/Ext Switch not in AUTO
PLL ALM LED	LED lights RED when phase lock loop is unlocked if switch in Auto or Ext Ref
REF ALM LED	LED lights GREEN when external 10 MHz reference is present, RED if removed (< 0.2 Vp-p)
Other	
Size, Bench Top	4.7” wide X 1.75” high X 12.5” deep
Size, Rack Mount (-R)	19 inch standard chassis 1.75”high X 13.0” deep (Option -R)
Power	+15VDC, 180 ma; -15VDC, 60ma; via 115 VAC wall power supply

*+10 to +40 degrees C; Specifications subject to change without notice

2.0 Installation

2.1 Mechanical - The 2099 PCB is packaged in an aluminum extrusion. The 2099 can be mounted on a 1 3/4" X 19" panel (option -R) that can be mounted to a rack using the 4 holes at the ends. The unit derives ± 15V from the wall power supply. Option -C is the unit without power supply for use with external switching power supply, Model 2000-01. See Figure 2.1

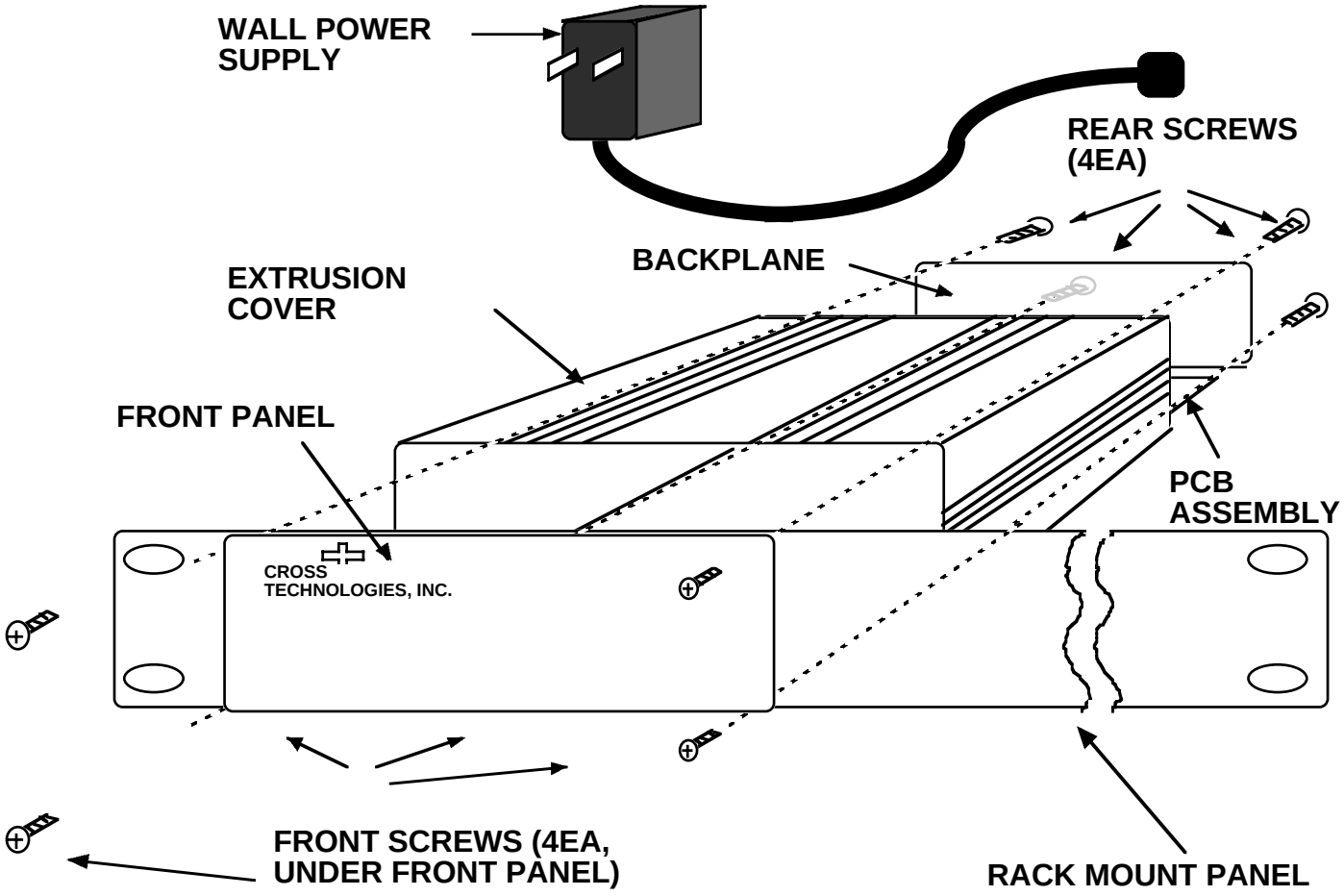

FIGURE 2.1 SERIES 2099 ASSEMBLY DRAWING (-R OPTION SHOWN)

2.2 Controls and Indicators - Figure 2.2 shows front panel controls and indicators.

2.3 Input / Output Signals - Figure 2.3 shows the input and output signals to the 2099-42. Table 2.1 is a description of the connectors and J4 pin functions.

2.4 Jumper Settings - Figure 2.4 and Table 2.2 show jumpers and other on-card controls.

2.4.1 Removing the Printed Circuit Board (PCB) From the Extrusion - To remove and re-install the printed circuit board (PCB) from the extrusion:

1.) **Always remove power** when removing or installing the PCB in to the extrusion.

2.) **PCB REMOVAL** - Remove four (4) **rear panel screws** (see Figure 2.1).

3.) **Gently** pull the backplane and PCB assembly completely out of the extrusion.

4.) **PCB INSTALLATION** -Make sure the shield goes in the lower channel and the PCB in the next channel above that in the extrusion.

5.) **Gently** push the backplane and PCB assembly completely in to the extrusion.

6.) Install four (4) **rear panel screws**.

2.5 Installation / Operation -

2.5.1 Initial Operation -

1.) If different from factory settings (Table 2.2), set on-card jumpers as desired (Figure 2.4)

2.) Connect the wall power supply to the 2099 and the wall power supply to 115 VAC, 60 Hz (Fig. 2.1)

3.) Connect a 1 V P-P 10 MHz signal to J1,10 MHz SIGNAL IN (Figure 2.1, Figure 2.3)

4.) Be sure S1 is in the center (AUTO) position (Figure 2.2)

5.) Be sure DS1 and DS4 are off and DS2 and DS3 are green (Figure 2.2).

6.) If needed, R20 can be adjusted (Figure 2.2) to SLIGHTLY adjust the internal VCXO frequency with S1 in the INTERNAL REF position and monitoring TP1. ALWAYS be sure S1 is in AUTO (center) for normal operation.

2.5.2 Switch S1 (Figure 2.2) - S1 selects between Internal Ref / AUTO / External Ref and operates as follows:

External Reference - This is a manual over ride of the AUTO position which forces the 2099-42 to always control the internal VCXO by locking it to the external 10 MHz reference. If in this position and the 10 MHz is removed, the PLL will lose lock and may force the internal VCXO to the high or low rail which causes it to be up to plus or minus 1.2 kHz from center frequency. No auto switch over to internal control of the VCXO will occur in this mode. The front panel potentiometer, R20 does NOT control the VCXO in this mode. Normal operation in this mode will have DS1 red, DS2 and DS3 green, and DS4 off (Figure 2.2).

AUTO - This forces the 2099-42 to always control the internal VCXO by locking it to the external 10 MHz reference if it is present. If in this position and the 10 MHz is removed, the PLL will lose lock and will force the internal VCXO to have the frequency set by front panel potentiometer, R20. R20 DOES control the VCXO in this mode if it has automatically switched to Internal. Normal operation in this mode will have DS1 and DS4 off and DS2 and DS3 green (Figure 2.2).

Internal Reference - This is a manual over ride of the AUTO position which forces the 2099-42 to always control the internal VCXO by front panel potentiometer, R20. R20 is a ten turn potentiometer which can control the VCXO by up to plus or minus 300 Hz from center frequency. If the 10 MHz external reference is present, the PLL Alarm LED, DS4 does not generally light in this mode but will flash occasionally, the rate of which is a rough indication of the offset of the VCXO from the reference frequency. The slower the rate of the flash, the closer the VCXO frequency is to the 10 MHz reference. No auto switch over to internal control of the VCXO will occur in this mode. As mentioned previously, the front panel potentiometer, R20 DOES control the VCXO in this mode. Normal operation in this mode will have DS1 red, DS2 red, DS3 green, and DS4 off and occasionally red for short flashes (Figure 2.2).

2.5.3 Selecting Clock Frequencies - The output clock frequencies are selected by the jumper on JP4 for Clock A and JP5 for Clock B. Setting this jumper closest to the front of the PCB selects 256, then moving it to the rear selects 192, 128, 96 and 64. The jumper position closest to the back of the PCB is not used.

2.5.4 Selecting 10 MHz Interface Parameters - Jumper JP2 selects the input termination of the external 10 MHz reference to either 75Ω termination (JP2 in DOT, factory setting) or 2 KΩ (JP2 in NON-DOT).

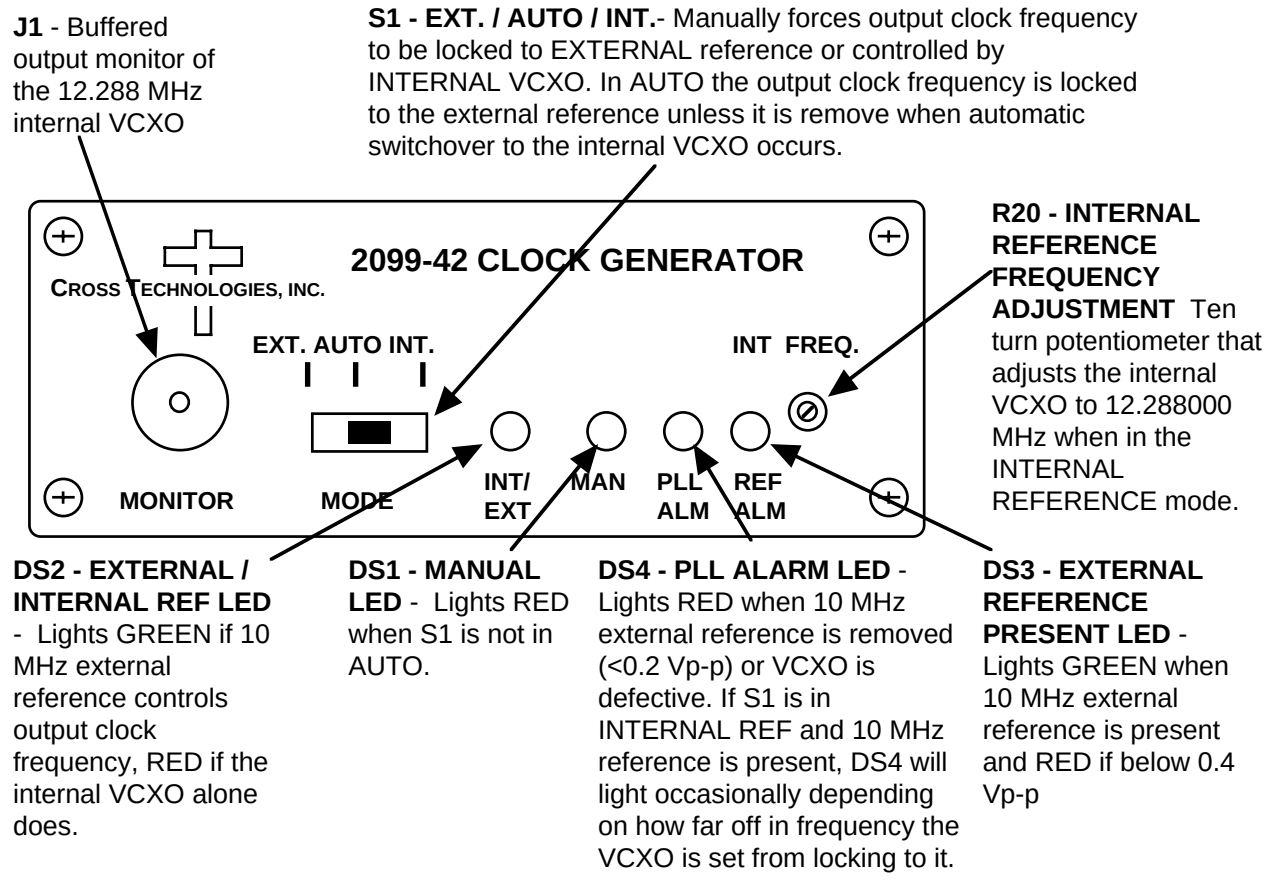

FIGURE 2.2 2099-42 Front Panel Controls and Indicators

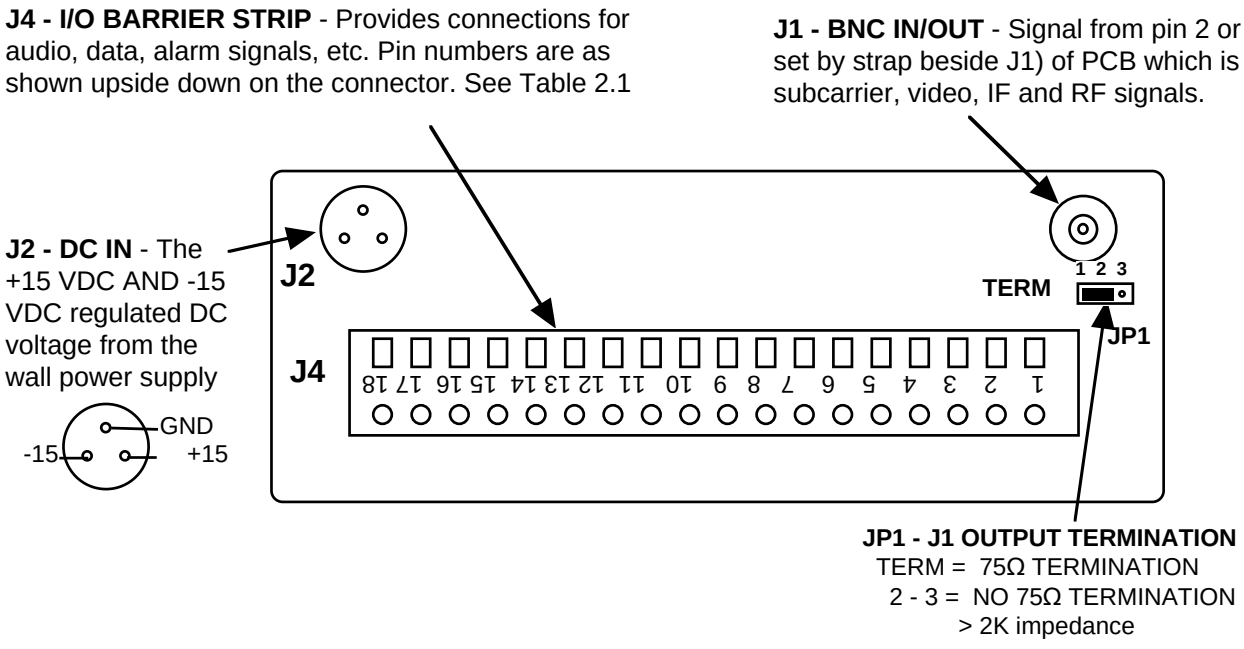

FIGURE 2.3 2099 Inputs and Outputs

TABLE 2.1 INPUT AND OUTPUT SIGNALS		
CONNECTOR	2099 FUNCTION	COMMENTS
J1	10 MHz INPUT	0.5 TO 1.5 V P-P (-4 to +6 dBm into 75 ohms)
J2	DC IN	± 15 VDC, 3PIN MINI-DIN
J3	PCB EDGE CONNECTOR	INTERNAL USE
J4 - PIN		
1	GROUND	
2	75Ω or 2 KΩ, 10MHz Signal In	Impedance electable by jumper JP1 on rear panel)
3	NOT USED	
4	RS422 Clock A Out (+)	One end of RS422 Clock A output
5	RS422 Clock A Out (-)	One end of RS422 Clock A output
6	NOT USED	
7	NOT USED	
8	+15 VDC Backup In	180 ma max,
9	+15 VOLTS.	180 ma max, from J2 Main Power Supply
10	MAJOR Alarm relay output	Open or short (selectable) to pin 12 if PLL alarm or no 10 MH
11	-15 VOLTS	60 ma max, from J2 Main Power Supply
12	MAJOR Alarm relay output	Open or short (selectable) to pin 10 if PLL alarm or no 10 MH
13	NOT USED	
14	-15 VDC Backup In	60 ma max
15	MANUAL ALARM OPEN COLLECTOR	Shorts to ground (+30 VDC,100 ma max) if S1 not in AUTO
16	RS422 Clock B OUT (+)	One end of RS422 Clock B output
17	RS422 Clock B OUT (-)	One end of RS422 Clock B output
18	GROUND	

TABLE 2.1 2099-42 Inputs and Outputs

TABLE 2.2 JUMPER DESCRIPTION					
JP#	Description	Dot	Non-dot	Normal	COMMENTS
JP3	ALARM RELAY POSITION	NO	NC	DOT	SELECTS NON ENERGIZED (No Alarm) POSITION OF MAJOR ALARM RELAY CLO
JP4	CLOCK B FREQUENCY	N/A	N/A	N/A	JUMPER POSITION SELECTS 64 TO 256 CLOCK FREQUENCY, CH A
JP5	CLOCK A FREQUENCY	N/A	N/A	N/A	JUMPER POSITION SELECTS 64 TO 256 CLOCK FREQUENCY, CH B

TABLE 2.2 JUMPER DESCRIPTIONS

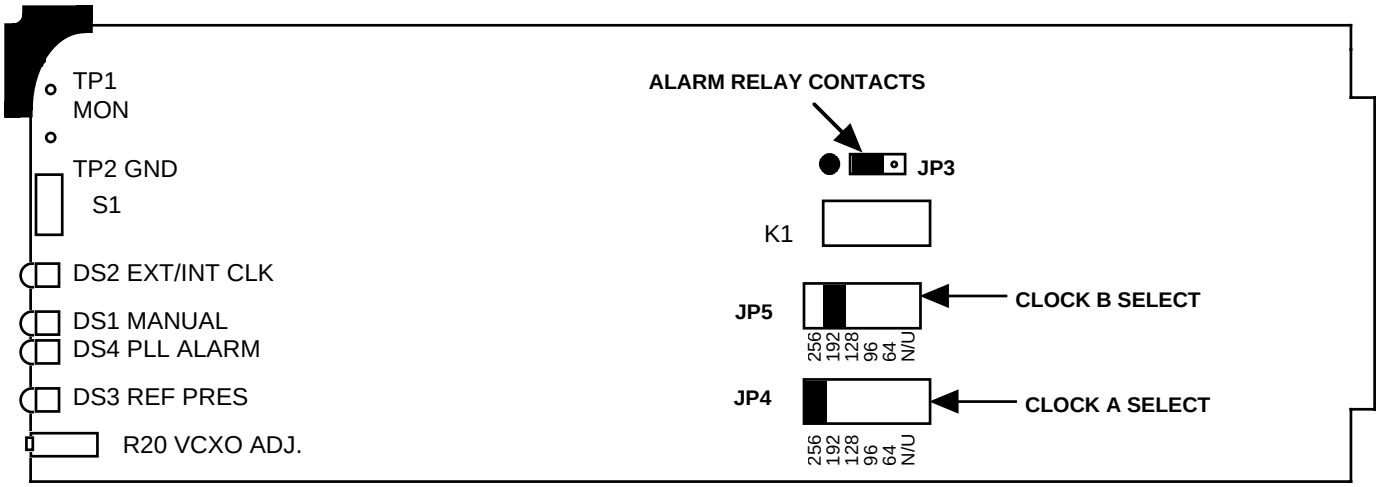

FIGURE 2.4 2099-42 On-Card Jumpers and Controls

3.0 Circuit Description

3.1 Block Diagram Discussion - 2099-42 (Figure 3.1) - The 10 MHz external reference signal goes to buffer amplifier U15 and then to U1 which squares up the incoming 10 MHz signal. This reference signal then goes to the synthesizer IC U2. U2 is programmed by controller U3 which provides data required for the synthesizer to function. The VCXO U5 provides the other input signal into the synthesizer U2. This is controlled through a switch consisting of U10 which determines whether the PLL is closed through loop amplifier U4 or if the frequency of the VCXO is determined by the front panel potentiometer R20 which sets the VCXO frequency when phase lock is broken or the external reference frequency has been removed. The output of U5, the VCXO also goes through buffer U6 and Q2 to a front panel test point TP1 for monitoring this frequency. The 12.288 Mhz output of the VCXO also goes to divider U9, U11, and U12. The outputs of U11 and U12 provide the clock signals at 64, 128, 256, 96, and 192 kHz. These signals go to jumpers JP4 and JP5 which are used to select the desired output clock frequency. These signals go to RS422 driver U14 to provide the clock A and clock B RS422 outputs.

The external 10 MHz reference frequency also goes to buffer amplifier U7 which drives peak detector CR8 and then goes to op amp U8, the output of which provides a +5 signal if the 10 MHz signal is present and a 0 volt signal if not present. This logic signal goes to switch S1 which selects manual, internal, external, or automatic mode. The output of S1 drives analog switch U10 through which the controls for the VCXO are routed. The output of S1 also goes to the manual indication LED DS1 and U6, a buffer amplifier which drives open collector output through Q1. The reference present signal out of U8 also goes to U13 which drives the reference alarm LED DS3. The output of the switch also goes to U13 which drives the red/green external/internal clock LED DS2. The lock detect output out of U2 goes to diode CR6 which detects the incoming signal which is a non-DC signal if the loop is out of lock. Presence of this AC signal is detected by U16 which drives DS4, the PLL alarm LED and also provides the PLL alarm signal which is diode OR'd with the reference present signal to drive Q3, the FET, which enables the relay K1 which provides contact closures indicating presence of a major alarm.

Regulators VR2 and VR1 provide +12 and -12 volts from the diode OR'd ±15V input and VR3 provides +5V for the logic circuitry.

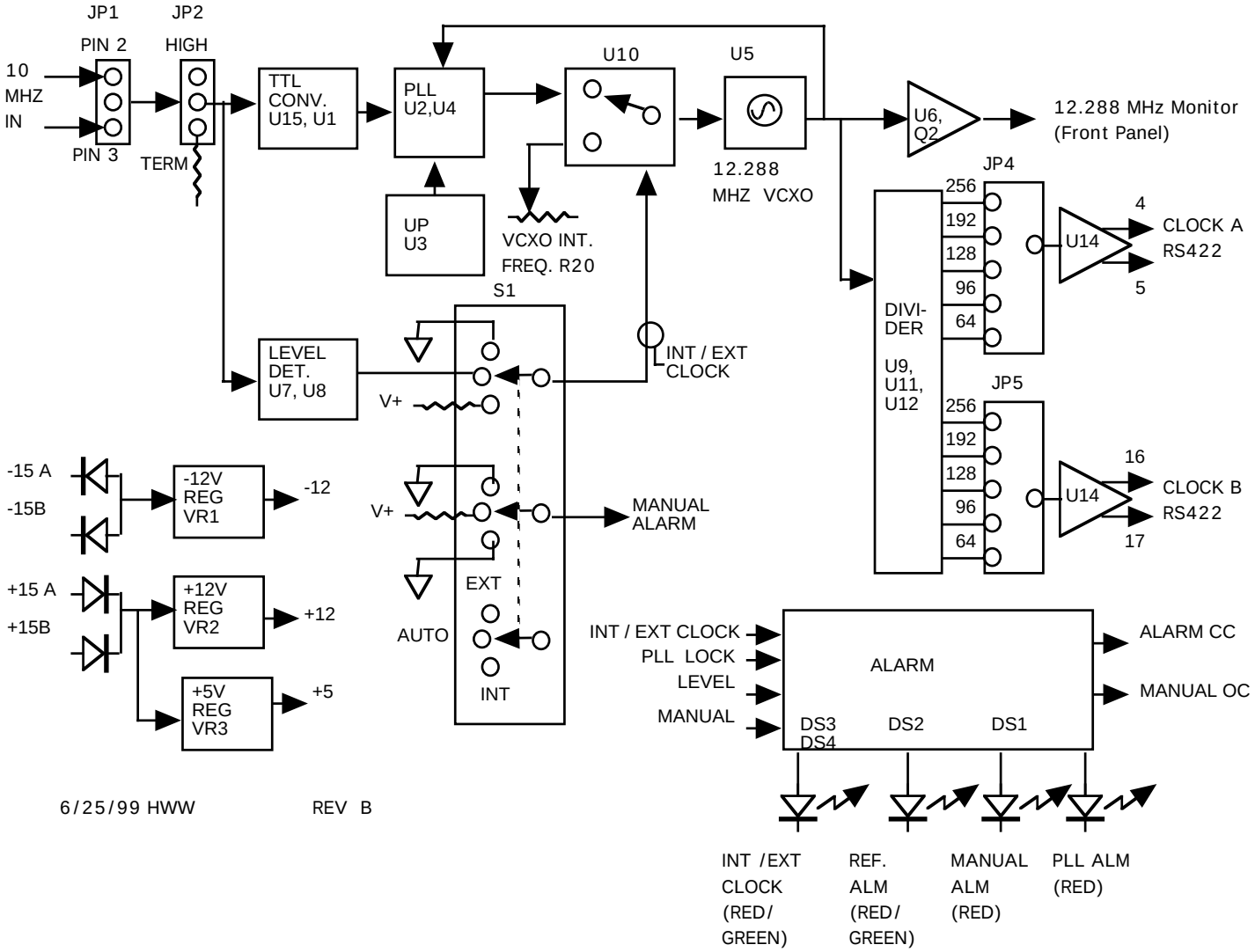

FIGURE 3.1 2099-42 BLOCK DIAGRAM